A product specification entitled "IMAGINE: The Image Engine -- Documentation & User's Manual" (version 2.80), provides additional details of embodiments of the data processing circuit 1 and is incorporated herein by reference and is appended as an annex to this specification.

IN THE CLAIMS:

Please cancel claims 1-3, 5-17 and 21-25 without prejudice.

Please add the following new claims:

26. (New) A processor comprising:

a plurality of functional units;

a bus structure including a plurality of buses, including a bus for each of the functional units; and

a plurality of bus registers, each coupled to an output of only a corresponding one of the plurality of functional units and to only a corresponding one of the plurality of buses.

27. (New) A processor as recited in claim 26, wherein the plurality of functional units comprises:

a multiplier unit; and

an arithmetic logic unit (ALU);

such that a first bus register of the plurality of bus registers is coupled to an output of the multiplier and to a first bus of the plurality of buses, and a second bus register of the plurality of bus registers is coupled to an output of the ALU and to a second bus of the plurality of buses.

28. (New) A processor as recited in claim 27, wherein the multiplier unit and the ALU are each adjustable to operate upon data words of any of a plurality of different lengths, the plurality of different lengths being integer multiples of each other.

29. (New) A processor as recited in claim 28, wherein the data words are integer data words.

30. (New) A processor as recited in claim 29, wherein the plurality of different lengths are multiples of eight bits.

31. (New) A processor as recited in claim 28, wherein the ALU has at least three operand inputs.

32. (New) A processor as recited in claim 31, further comprising a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving a plurality of bits from the control register to execute the three port parametrised logic function.

33. (New) A processor as recited in claim 27, wherein the plurality of functional units further comprises a shift register, such that a third bus register of the plurality of bus registers is coupled to an output of the shift register and to a third bus of the plurality of buses.

34. (New) A processor as recited in claim 33, wherein the plurality of functional units further comprises a register bank including a plurality of registers on which operations are to be performed, such that a fourth bus register is coupled to a first one of the plurality of registers and to a fourth bus of the plurality of buses, and a fifth bus register is coupled to a second one of the plurality of registers and to a fifth bus of the plurality of buses.

35. (New) A processor comprising:

a multiplier unit adjustable to multiply integer data words of any of a plurality of different lengths, the plurality of different lengths being integer multiples of each other;

an arithmetic logic unit (ALU) adjustable to perform arithmetic operations on integer data words of any of the plurality of different lengths;

a shift register;

a bus structure including a plurality of buses, including a bus for each of the multiplier unit, the ALU, and the shift register; and

a plurality of bus registers, each coupled to an output of a separate corresponding one of the multiplier unit, the ALU, and the shift register and to a separate corresponding one of the plurality of buses.

#10 36. (New) A processor as recited in claim 35, wherein the plurality of different lengths are multiples of eight bits.

37. (New) A processor as recited in claim 35, wherein the ALU has at least three operand inputs.

38. (New) A processor as recited in claim 37, further comprising a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving a plurality of bits from the control register to execute the three port parametrised logic function.

39. (New) A processor as recited in claim 35, wherein the plurality of functional units further comprises a register bank including a plurality of registers on which operations are to be performed by the multiplier, the ALU or the shifter, and wherein the plurality of bus registers includes a first bus register coupled to a first one of the plurality of registers in the register bank and to a first one of the plurality of buses, and a second bus register coupled to a second one of the plurality of registers in the register bank and to a second one of the plurality of buses.

40. (New) A circuit for processing integer data for graphic image processing applications, comprising:

a multiplier unit having a pipeline to multiply integer data words of 8 bits or multiples thereof, the pipeline being adjustable to the length of the integer data words to be multiplied;

an arithmetic logic unit (ALU) to perform arithmetic operations on integer data words of 8 bits or multiples thereof, the word length of the ALU being adjustable in accordance with the multiple of 8 bits constituting the integer data words;

a register unit including at least two registers to store integer data words on which a multiplication or arithmetic operation is to be performed; and

a bus structure including a plurality of buses, including a bus for each of the multiplier, the ALU, and each of the at least two registers; and

a plurality of bus registers, each coupled to an output of a separate corresponding one of the multiplier, the ALU, and each of the at least two registers, and each coupled to a separate corresponding one of the plurality of buses.

41. (New) A circuit as recited in claim 40, further comprising a shift register, wherein the plurality of bus registers includes an bus register coupled to an output of the shift register and to a corresponding one of the plurality of buses.

42. (New) A circuit as recited in claim 41, wherein the ALU has at least three operand inputs.

43. (New) A circuit as recited in claim 42, further comprising a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving a plurality of bits from the control register to execute the three port parametrised logic function.